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EXAMINER	
NICELY, JOSEPH C	
ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/571,426	MORI ET AL.	
	Examiner	Art Unit	
	Joseph C. Nicely	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,6,7 and 11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6,7 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to the Request for Continued Examination filed 04/23/2009 in which claims 1, 3, 6, and 7 were amended, claims 8-10 cancelled, and claim 13 added.

2. Claims 1, 3, 6, 7, and 11-13 are currently pending.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 12 recites that the silicon film contains no impurities, which finds support in paragraph [0114]. The specification, however, fails to provide details as to how a silicon film can be formed with no impurities therein since the film deposition process inherently introduces some level of impurity. Impurities can be introduced by the ambient atmosphere during deposition, from the precursor gases themselves, or having been transferred or diffused from another region, e.g. the substrate, into the film. There is no disclosure in the application as to how all impurities are prevented from existing inside the silicon film and, therefore, there is insufficient information that would enable a person having ordinary skill in the art to make a silicon film that contains no impurities.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Examiner notes that an official translation of JP 200439832 A is included with this communication and is used as an English language equivalent for the rejections based upon the Japanese Patent document 200439832 A in the following rejections.

7. Claims 1, 3, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshiko (JP 2004-039832 and Yoshiko hereinafter).

As to claim 1: Yoshiko discloses **a solid state imaging apparatus comprising: a photoelectric conversion section** (section b of Fig. 1(a) and/or all of Fig. 2) **formed in an imaging area** (pixel region 37) **of a silicon substrate** (1)**, the photoelectric conversion section** (section b of Fig. 1(a); [0080]) **including: a surface layer** (19) **having a first conductivity type** (p-type) **provided on a top portion of the silicon substrate** (Fig. 2; [0059])**, a first semiconductor layer made of silicon** (18) **having a second conductivity type** (n-type)**, and serving as a charge accumulation region** ([0059], signal charge is accumulated in layer 18)**, and provided under the surface layer** (Fig. 2; [0059])**, and a second semiconductor layer made of silicon** (12) **having the first conductivity type** (p-type) **provided under the first semiconductor layer** (Fig. 2; [0059])**; an isolation region** (7b) **formed in at least one part of the silicon substrate located around the photoelectric conversion section** (Fig. 2;

[0057]), **the isolation region being made of a silicon film which fills an isolation trench formed on the semiconductor substrate** ([0092]; trench 4 is filled with silicon oxide 7a to form STI 7b after CMP; Examiner interprets "a silicon film" to mean a film comprising silicon, 7a is silicon oxide and thus explicitly comprises silicon)**; a first silicon layer made of silicon** (inner portion, portion closest to STI 7b, of layer 6) **having the first conductivity type** (p-type) **formed in a region of the silicon substrate, and forming the bottom and sidewalls of the isolation trench** (Figs. 2 and 5(d); [0019] and [0063]; Examiner interprets that a first portion (inner portion) of layer 6 comprises the first silicon layer and a second portion (outer portion) comprises the second silicon layer)**; and a second silicon layer made of silicon** (outer portion, portion furthest from STI 7b, of layer 6) **having the first conductivity type** (p-type) **in contact with a bottom side of the first silicon layer** (Figs. 2 and 5(d); [0019] and [0063]; as the only claimed difference between the first and second silicon layers is placement, Examiner interprets that a first portion (inner portion) of layer 6 comprises the first silicon layer and a second portion (outer portion) comprises the second silicon layer)**, wherein the photoelectric conversion section** (section b of Fig. 1(a) and/or all of Fig. 2) **is in contact with the isolation region** (7b)**, the first silicon layer** (inner portion of layer 6)**, and the second silicon layer** (outer portion of layer 6)**, and a depth of the first semiconductor layer** (18) **is substantially the same as that of the second silicon layer** (Fig. 2; second silicon layer corresponds to a second (outer) portion of layer 6, which Figure 2 shows as being at the same depth as the deepest depth of layer 18).

8. As to claim 3: Yoshiko discloses **an insulating film** (5) **covering the bottom and sidewalls of the isolation trench** (Fig. 5(c); [0089]).

9. As to claim 13: Yoshiko discloses **where the second silicon layer is in contact with a side surface of the first semiconductor layer** (Fig. 2; second silicon layer corresponds to a second (outer) portion of layer 6; layer 6 has a vertical and a horizontal section and the outer portion is in direct contact with the first semiconductor layer 18).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 1, 3, 6, 7, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiko in view of Mouli (US 7,492,027 and Mouli hereinafter).

As to claim 1: Yoshiko discloses **a solid state imaging apparatus comprising: a photoelectric conversion section** (section b of Fig. 1(a) and/or all of Fig. 2) **formed in an imaging area** (pixel region 37) **of a silicon substrate** (1)**, the photoelectric conversion section** (section b of Fig. 1(a); [0080]) **including: a surface layer** (19) **having a first conductivity type** (p-type) **provided on a top portion of the silicon substrate** (Fig. 2; [0059])**, a first semiconductor layer made of silicon** (18) **having a second conductivity type** (n-type)**, and serving as a charge accumulation region** ([0059], signal charge is accumulated in layer 18)**, and provided under the surface layer** (Fig. 2; [0059])**, and a second semiconductor layer made of silicon** (12) **having the first conductivity type** (p-type) **provided under the first semiconductor layer** (Fig. 2; [0059])**; an isolation region** (7b) **formed in at least one part of the silicon substrate located around the photoelectric conversion section** (Fig. 2; [0057])**, the isolation region being made of a film which fills an isolation trench formed on the semiconductor substrate** ([0092]; trench 4 is filled with silicon oxide 7a to form STI 7b after CMP)**; a first silicon layer made of silicon** (inner portion, portion closest to STI 7b, of layer 6) **having the first conductivity type** (p-type) **formed in a region of the silicon substrate, and forming the bottom and sidewalls of the isolation trench** (Figs. 2 and 5(d); [0019] and [0063]; Examiner interprets that a first portion (inner portion) of layer 6 comprises the first silicon layer and a second portion (outer portion) comprises the second silicon layer)**; and a second silicon layer made**

of silicon (outer portion, portion furthest from STI 7b, of layer 6) **having the first conductivity type** (p-type) **in contact with a bottom side of the first silicon layer** (Figs. 2 and 5(d); [0019] and [0063]; Examiner interprets that a first portion (inner portion) of layer 6 comprises the first silicon layer and a second portion (outer portion) comprises the second silicon layer)**, wherein the photoelectric conversion section** (section b of Fig. 1(a) and/or all of Fig. 2) **is in contact with the isolation region** (7b)**, the first silicon layer** (inner portion of layer 6)**, and the second silicon layer** (outer portion of layer 6)**, and a depth of the first semiconductor layer** (18) **is substantially the same as that of the second silicon layer** (Fig. 2; second silicon layer corresponds to a second (outer) portion of layer 6, which Figure 2 shows as being at the same depth as the deepest depth of layer 18).

Yoshiko fails to expressly disclose where the film comprising the isolation region is **a silicon film** which fills an isolation trench.

In the same field of endeavor, Mouli discloses where the film comprising the isolation region is **a silicon film** which fills an isolation trench (Fig. 3C; col. 5, lines 19-26; silicon film 205 can be polysilicon (doped or undoped); trench is formed to a desired depth in the substrate).

Given the teachings of Mouli, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Yoshiko by employing the well known or conventional features of STI formation in an image sensor, such as displayed by Mouli, by employing a polysilicon film in a STI trench of a desired depth in order to provide a trench material that are more

easily deposited into trenches of various depths (col. 4, lines 3-10) and provides enhanced isolation that prevents crosstalk.

13. As to claim 3: Yoshiko combined with Mouli discloses **an insulating film** (5) **covering the bottom and sidewalls of the isolation trench** (Fig. 5(c); [0089]).

14. As to claim 6: Yoshiko combined with Mouli discloses **a MOS transistor** (51) **formed in the imaging area** (Fig. 1(a); imaging area is pixel region 37). Yoshiko in view of Mouli fails to expressly disclose **where the silicon film isolation material contains an impurity of the opposite conductivity type to source and drain regions of the MOS transistor.** Yoshiko discloses have source and drain regions in Fig. 1(a), but fails to expressly disclose the conductivity type. Mouli discloses in col. 5, lines 19-26 that the polysilicon film can comprise n or p type impurities. Therefore, the claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since, as stated in KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007), a person having ordinary skill has good reason to pursue the known options within his or her technical grasp, in the instant case there are only two types of conductivity types for the source and drain regions (and for the doped polysilicon layer), n or p type as listed by Mouli; if this leads to the anticipated success, in the instant case a film with desired electrical properties, it is likely the product not of innovation but of ordinary skill and common sense. In any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular claimed dopant arrangement because applicant has not disclosed that the limitations are for a particular

unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another conductivity type. Further, given the teachings of Mouli, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Yoshiko by employing the well known or conventional features of STI formation in an image sensor, such as displayed by Mouli, by employing a polysilicon film in a STI trench of a desired depth in order to provide a trench material that are more easily deposited into trenches of various depths (col. 4, lines 3-10) and provides enhanced isolation that prevents crosstalk.

15. As to claim 7: Yoshiko in view of Mouli discloses **where the silicon film isolation material is made of amorphous silicon, polycrystalline silicon or porous silicon** (Fig. 3C; col. 5, lines 19-26; silicon film 205 can be polysilicon (doped or undoped); trench is formed to a desired depth in the substrate)**.** Given the teachings of Mouli, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Yoshiko by employing the well known or conventional features of STI formation in an image sensor, such as displayed by Mouli, by employing a polysilicon film in a STI trench of a desired depth in order to provide a trench material that are more easily deposited into trenches of various depths (col. 4, lines 3-10) and provides enhanced isolation that prevents crosstalk.

16. As to claim 11: Yoshiko in view of Mouli fails to expressly disclose **a camera comprising the solid state imaging apparatus according to Claim 1.** However, it

would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the solid stat imager as taught by Yoshiko in view of Mouli and detailed in paragraph 11 in a camera as it is a well known technique in the art to use solid state devices as imaging apparatuses in cameras and the application of which is recognized to be within the ordinary capabilities of one skilled in the art and would have yielded the predictable results of a solid state imaging device with reduced dimension size ([0024]), increased imaging capabilities, and decreased crosstalk occurrence using a trench filling material that is easily deposited into trenches of various size. KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007).

17. As to claim 13: Yoshiko combined with Mouli discloses **where the second silicon layer is in contact with a side surface of the first semiconductor layer** (Fig. 2; second silicon layer corresponds to a second (outer) portion of layer 6; layer 6 has a vertical and a horizontal section and the outer portion is in direct contact with the first semiconductor layer 18)**.**

18. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiko in view of Mouli as applied to claim 1 above, and further in view of Zehavi et al (US 6,583,377 and Zehavi hereinafter).

Although the method disclosed by Yoshiki in view of Mouli shows substantial features of the claimed invention (discussed in paragraph 12 above), it fails to expressly disclose:

where the silicon material contains no impurities.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Yoshiko in view of Mouli, as evidenced by Zehavi.

Yoshiko in view of Mouli disclose using polysilicon in the trench structures. Zehavi in col. 1, lines 38-64 states that a pure form (Examiner interprets pure in its plain meaning, i.e., a structure free of anything of a different or contaminating kind) of silicon is virgin polysilicon. Zehavi further discloses that it is desirable that the silicon film, i.e., virgin polysilicon, be of very high purity, with impurity levels being far less than 1% atomic. Therefore, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular claimed impurity level because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another low level of impurity (e.g. less than 1% atomic).

Given the teachings of Zehavi, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Yoshiko in view of Mouli by employing the well known or conventional features of semiconductor-grade polysilicon layer formation, such as displayed by Zehavi, by employing a polysilicon layer that is in contact with the substrate to possess low or no impurities in order to prevent impurities from the polysilicon layer from diffusing into the substrate and degrading its semiconductor characteristics.

Response to Arguments

19. Applicant's arguments filed 04/23/2009 have been fully considered but they are not persuasive.

20. In the remarks, applicant argues in substance that:

1) The STI structure of Yoshiko is made of silicon oxide but not a silicon film.

2) Yoshiko, or other cited references (page 5 of arguments lists the other cited references, i.e., Seo (2004/0048444), Williams et al (US 6,900,091, and Lee (US 2004/0127035)), fails to recognize or suggest the issue relating to the stress-induced defects due to the difference of the thermal expansion coefficients between the isolation region and the substrate and there is therefore no motivation or suggestion to combine Yoshiko with any of the other cited references.

3) None of the cited references (page 5 of arguments lists the other cited references, i.e., Seo (2004/0048444), Williams et al (US 6,900,091, and Lee (US 2004/0127035)) disclose or suggest that the depth of the first semiconductor layer is substantially the same as that of the second silicon layer.

21. Examiner respectfully traverses applicant's remarks:

a. As to point 1), claim 1 recites that "the isolation region [is] made of a silicon film". The broadest reasonable interpretation taken by the Examiner for the term "a silicon film" is a film that comprises silicon. The STI structure of Yoshiko comprises silicon oxide, which explicitly comprises silicon, and is thus a silicon film. Applicant has failed to provide an explicit definition for the term "a

silicon film" and, in accordance with MPEP 2106, claims must given their broadest reasonable interpretation in light of the supporting disclosure without importing limitations from the specification unnecessarily.

b. As to point 2), in response to applicant's argument that none of the references cited (Office action mailed 01/23/2009 and the list of cited references summarized by applicant on page 5 of the response filed 04/23/2009) recognize or suggest the issue relating to the stress-induced defects due to the difference of the thermal expansion coefficients between the isolation region and the substrate, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

c. As to point 3), there is no claimed difference between the first and second silicon layer. Both first and second silicon layers comprise silicon and comprise the same conductivity type. Therefore, the broadest reasonable interpretation taken by the Examiner is that the silicon layer 6 of Yoshiko comprises two regions, a first inner region that comprises the first silicon layer and a second outer region that comprises the second silicon layer. As pointed out by the applicant on page 7 of the remarks submitted 04/23/2009, the first semiconductor layer 18 has substantially a same depth as a lower portion of the silicon layer 6, which corresponds to the second silicon layer region of layer 6.

22. Applicant's arguments with respect to claims 1, 3, 6, 7, and 11-13 have been considered but are moot in view of the new ground(s) of rejection, see paragraphs 11-

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph C. Nicely whose telephone number is (571) 270-3834. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joseph C. Nicely/
Examiner, Art Unit 2813

/Matthew C. Landau/
Supervisory Patent Examiner, Art Unit 2813